Listing of Claims

This listing of the claims will replace all prior versions, and listings, of claims in the application:

1. (original) A logic device, comprising:

a plurality of interconnecting carbon nanotube devices, wherein said interconnecting carbon nanotube devices comprise a plurality of electrically connected carbon nanotubes on one or more levels of a substrate, and wherein said carbon nanotubes are formed within at least one nanosized catalyst retaining structure in said substrate.

2. (original) The logic device of Claim 1, further comprising one or more electrical bond pads coupled to the plurality of carbon nanotube devices and configured to provide external electrical connections to the logic device.

3. (original) The logic device of Claim 1, wherein said plurality of interconnecting carbon nanotube devices is electrically connected via patterned electrically conducting films.

4. (original) The logic device of Claim 1, wherein said plurality of interconnecting carbon nanotube devices is electrically connected via patterned electrically conducting carbon nanotubes.

5. (original) The logic device of Claim 1, wherein said plurality of interconnecting carbon nanotube devices are electrically connected via a combination of patterned electrically conducting films and patterned electrically conducting carbon nanotubes.

6. (original) The logic device of Claim 3, wherein said patterned electrically conducting films are metallic films.

7. (original) The logic device of Claim 1, wherein a plurality of carbon nanotube devices are formed on a single carbon nanotube and wherein said plurality of carbon nanotube devices are electrically isolated by nonconducting segments of said single carbon nanotube.

8. (original) The logic device of Claim 2, wherein said electrical bond pads comprise metallic bond pads.

9. (original) The logic device of Claim 8, wherein said metallic bond pads are lithographically fabricated.

10. (original) The logic device of Claim 1, wherein said device is fabricated on a doped silicon substrate.

11. (original) The logic device of Claim 1, wherein said device is fabricated on an aluminum substrate.

12. (original) The logic device of Claim 1, wherein said device is fabricated on a substrate suitable for electrochemical etching.

13. (original) The logic device of Claim 12, wherein said substrate further comprises metal interconnects coupled to said carbon nanotube devices.

14. (original) The logic device of Claim 12, wherein said substrate comprises layers of doped crystalline silicon and patterned metal interconnects.

15. (original) The logic device of Claim 12, wherein said substrate is fabricated by stacking of deposited metal lines and epitaxialy grown or deposited silicon layer, followed by ion implantation and recrystallization of the silicon.

16. (original) The logic device of Claim 12, wherein said substrate further comprises a plurality of layers bonded together.

17. (original) The logic device of Claim 11, wherein said substrate further comprises layers of aluminum and patterned metal interconnects fabricated by stacking deposited metal lines and recrystallized deposited aluminum.

18. (withdrawn) A method of fabricating a carbon nanotube device, comprising the steps of:

fabricating a template of nanosized catalyst retaining structures within a substrate;
depositing catalyst within said nanosized catalyst retaining structures; and
synthesizing carbon nanotubes that conform to said template of said nanosized catalyst retaining structures.

19. (withdrawn) The method of Claim 18, wherein said template bounds a pattern of said carbon nanotube devices.

20. (withdrawn) The method of Claim 18, wherein said template bounds a length of said carbon nanotube devices.

21. (withdrawn) The method of Claim 18, wherein said template bounds a vertical profile of said carbon nanotube devices.

22. (withdrawn) The method of Claim 18, wherein said nanosized catalyst retaining structures comprise uniform holes used to synthesize vertical carbon nanotube interconnects and non-uniform holes used to synthesize carbon nanotube devices.

23. (withdrawn) The method of Claim 18, further comprising the step of interconnecting carbon nanotube devices with electrically conducting interconnects to form logic devices.

24. (withdrawn) The method of Claim 18, wherein said template is fabricated by etching said substrate at specified locations.

25. (withdrawn) The method of Claim 24, wherein said specified locations are patterned using lithographic techniques.

26. (withdrawn) The method of Claim 18, wherein fabricating said template comprises placing of an impurity, local defect, stress, or optical energy to initiate formation of said nanosized catalyst retaining structures.

27. (withdrawn) The method of Claim 22, wherein said non-uniform holes have discontinuities in diameter along a vertical axis of said holes.

28. (withdrawn) The method of Claim 27, wherein said template is generated using electrochemical etching or photo-electrochemical etching.

29. (withdrawn) The method of Claim 28, wherein said electrochemical etching process is varied by process parameters selected from the group consisting of current density, concentration of the etchant, doping of the silicon substrate, and luminescence.

30. (withdrawn) The method of Claim 29, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling said process parameters as a function of depth of penetration, etching rate and etching time.

31. (withdrawn) The method of Claim 29, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling a current flux as a function of time.

32. (withdrawn) The method of Claim 29, wherein said electrochemical etching of a doped silicon substrate is achieved with a diluted HF acid and current densities of 10 mA/ cm^2.

33. (withdrawn) The method of Claim 32, wherein said electrochemical etching is configured to produce a cylindrical template with a bulge or an hour-glass shaped template.

34. (withdrawn) The method of Claim 32, wherein said electrochemical etching is configured to produce a cylindrical template with a diameter between 1 and 50 nm.

35. (withdrawn) The method of Claim 28, wherein said substrate is an aluminum substrate, and wherein said electrochemical etching process is varied by process

parameters selected from the group consisting of current density and concentration of the etchant.

36. (withdrawn) The method of Claim 35, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling said process parameters as a function of depth of penetration, etching rate and etching time.

37. (withdrawn) The method of Claim 35, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling a current flux as a function of time.

38. (withdrawn) The method of Claim 35, wherein said electrochemical etching of a doped silicon substrate is achieved with a diluted HF acid and current densities of 10 mA/ cm^2.

39. (withdrawn) The method of Claim 35, wherein said electrochemical etching is configured to produce a cylindrical template with a bulge or an hour-glass shaped template.

40. (withdrawn) The method of Claim 35, wherein said electrochemical etching is configured to produce a cylindrical template with a diameter between 1 and 50 nm.

41. (withdrawn) The method of Claim 18, wherein catalyst comprises a metal catalyst.

42. (withdrawn) The method of Claim 41, wherein said metal catalyst is selected from the group consisting of Fe, Ni, and Co.

43. (withdrawn) The method of Claim 41, wherein said catalyst is deposited using chemical deposition or electro-deposition.

44. (withdrawn) The method of Claim 41, wherein said deposition of said metal catalyst is achieved concurrently with said fabrication of said template by incorporating a metal catalyst in an electrochemical etching solution.

45. (withdrawn) The method of Claim 44, wherein said etching solution comprises HF with traces of iron to introduce catalytic metal into said etching solution.

46. (withdrawn) The method of Claim 18, wherein synthesizing said nanotubes comprises thermal deposition of hydrocarbides using a CVD process.

47. (withdrawn) A method for manufacturing an array of transistors, comprising:
growing aligned carbon nanotubes within a catalyst retaining template; and
introducing one or more discontinuities within a structure of said carbon nanotubes, wherein said discontinuities are conductivity discontinuities along a vertical

axis of said carbon nanotubes, wherein if one discontinuity is introduced a diode is formed and if two discontinuities is introduced a transistor is formed.

48. (withdrawn) The method of Claim 47, wherein said discontinuities comprise variations in a diameter of said carbon nanotubes or impurities in said carbon nanotube.

49. (withdrawn) The method of Claim 48, wherein said variations in said diameter of said carbon nanotubes are achieved by varying an electrochemical etch process.

50. (withdrawn) The method of Claim 47, wherein said catalyst retaining structure is formed on a substrate.

51. (withdrawn) The method of Claim 47, wherein said at least two discontinuities comprise pentagon-heptagon pairs.

52. (withdrawn) The method of Claim 47, wherein more than at least two discontinuities are introduced within said structure of said carbon nanotube to produce one or more carbon nanotube transistors along said vertical axis.

53. (withdrawn) A carbon nanotube transistor, comprising:

a carbon nanotube with at least two defects in said carbon nanotube, and wherein said defects divide said carbon nanotube into three regions with differing conductivities.

54. (withdrawn) The carbon nanotube transistor of Claim 53, wherein said defects comprise variations in a diameter of said carbon nanotubes.

55. (withdrawn) The carbon nanotube transistor of Claim 54, wherein said variations in said diameter of said carbon nanotubes are achieved by varying an electrochemical etch process.

56. (withdrawn) The carbon nanotube transistor of Claim 53, wherein said catalyst retaining structure is formed within a substrate.

57. (withdrawn) The carbon nanotube transistor of Claim 53, wherein said at least two discontinuities comprise pentagon-heptagon pairs.

58. (withdrawn) The carbon nanotube transistor of Claim 53, wherein more than two discontinuities are introduced within said structure of said carbon nanotube to produce a plurality of carbon nanotube transistors along said vertical axis.

59. (original) A logic device, comprising:

a substrate;

a layer of insulating material in which at least one catalyst retaining structure is formed;

at least one carbon nanotube formed within said catalyst retaining structure, wherein said at least one carbon nanotube has at least two defects in said carbon nanotube, and wherein said defects divide said carbon nanotube into at least three regions with differing conductivities.

60. (original) The logic device of Claim 59, wherein said defects comprise variations in a diameter of said carbon nanotubes;

61. (original) The logic device of Claim 60, wherein said variations in said diameter of said carbon nanotubes are achieved by varying an electrochemical etch process.

62. (original) The logic device of Claim 59, wherein said catalyst retaining structure is formed on a substrate.

63. (original) The logic device of Claim 59, wherein said at least two discontinuities comprise pentagon-heptagon pairs.

64. (original) The logic device of Claim 59, wherein more than two discontinuities are introduced within said structure of said carbon nanotubes to produce a plurality of carbon nanotube transistors along said vertical axis.

65. (withdrawn) A CNMED comprising:

at least one vertically oriented carbon nanotube, wherein said vertically oriented carbon nanotube is created in a substrate; and

at least one horizontal interconnect layer, wherein interconnects in said interconnect layer electrically connect said vertically oriented carbon nanotube.

66. (previously presented) A patterned array comprising:
a plurality of CNMEDs;

wherein each said CNMED includes at least one carbon nanotube; and

wherein said CNMEDs are located according to the location of templates in a substrate layer.

67. (previously presented) A template in a substrate, said template being adapted to contain and determine the shape of a carbon nanotube as the carbon nanotube is created.

68. (previously presented) The template of claim 67, wherein said template has been oxidized.

69. (previously presented) The template of claim 67, wherein said template has been nitridized.

70. (previously presented) The template of claim 67, wherein said template is at least partially electrically isolated from the substrate.

71. (previously presented) A carbon nanotube in a substrate, said carbon nanotube having been created in a template such that the shape of the carbon nanotube conforms to the shape of the template.

72. (previously presented) The carbon nanotube of claim 71, wherein the template has been oxidized.

73. (previously presented) The carbon nanotube of claim 71, wherein the template has been nitridized.

74. (previously presented) The carbon nanotube of claim 71, wherein the template is at least partially electrically isolated from the substrate.

75. (withdrawn) A process of creating a carbon nanotube comprising:
creating a template in a substrate, wherein the template has a template shape; and
creating a carbon nanotube in the template, wherein the shape of the carbon nanotube conforms to the template shape.

76. (withdrawn) A method of creating a carbon nanotube comprising:
creating a template within a substrate; and
creating the carbon nanotube in the template, wherein the shape of the carbon nanotube conforms to the shape of the template.

77. (withdrawn) A process of etching a template comprising:
designating etching process parameters to achieve a desired template shape; and
etching the template within a substrate, wherein the etching process parameters are used to control the template's shape.

78. (withdrawn) The process of claim 77, wherein control of the template's shape comprises control of the template's diameter along its depth.

79. (withdrawn) The process of claim 77, wherein said etching the template comprises etching the template electrochemically.

80. (withdrawn) The process of claim 77, wherein said etching the template comprises etching the template photoelectrochemically.

81. (withdrawn) The process of claim 77, wherein the substrate material comprises a member of the class consisting of silicon, aluminum, and gallium arsenide.

82. (withdrawn) The process of claim 77, further comprising:
oxidizing the template.

83. (withdrawn) The process of claim 77, further comprising:
nitridizing the template.

84. (withdrawn) The process of claim 77, further comprising:
processing the template so that the template is at least partially electrically isolated from the substrate.

85. (withdrawn) The process of claim 84, wherein processing the template comprises oxidizing the template.

86. (withdrawn) The process of claim 84, wherein processing the template comprises nitridizing the template.

87. (withdrawn) The process of claim 77, wherein said etching is performed using etchant, and wherein the etching process parameters are a function of the depth of penetration of the etchant.

88. (withdrawn) The process of claim 87, wherein the etchant comprises diluted hydrofluoric acid.

89. (withdrawn) The process of claim 77, wherein the template comprises a plurality of segments, and wherein at least two template segments with different shapes are created in series.

90. (withdrawn) The process of claim 77, wherein the template comprises a plurality of segments, and wherein at least two template segments are created in parallel, whereby the template shape includes at least two branches.

91. (withdrawn) The process of claim 77, wherein said etching includes:
applying current flux to etch the substrate; and
controlling the current flux as a function of time, wherein the shape of the template is determined at least in part by the current flux.

92. (previously presented) A template in a substrate, wherein said template has a shape including at plurality of template segments, and wherein at least two of the template segments have different shapes.

93. (previously presented) The template of claim 92, wherein the difference of shape between the at least two of the template segments comprises a difference of diameters along said template's vertical axis.

94. (previously presented) A template in a substrate, wherein said template has a shape including at least two different branches, whereby each of at least two of the branches have a unique vertical axis relative to the other.

95. (previously presented) A carbon nanotube in a substrate, wherein said template has a shape including at plurality of carbon nanotube segments, and wherein at least two of the carbon nanotube segments have different shapes.

96. (previously presented) The carbon nanotube of claim 92, wherein the difference of shape comprises a difference of diameters along said carbon nanotube's vertical axis.

97. (previously presented) A carbon nanotube in a substrate, wherein said carbon nanotube has a shape including at least two different branches, whereby each of at least two of the branches have a unique vertical axis relative to the other.

98. (withdrawn) A process of etching a substrate comprising:
providing an upper substrate layer;
providing a lower substrate layer;
providing a metal layer below the upper substrate layer and above the lower substrate layer;
etching a template such that the template penetrates the upper substrate layer, the metal layer, and the lower substrate layer.

99. (withdrawn) The process of claim 98, wherein the metal layer comprises patterned lines.

100. (withdrawn) The process of claim 98, wherein the metal layer comprises a blanket deposit.

101. (previously presented) A template penetrating an upper substrate layer, a metal layer, and a lower substrate layer,
wherein the metal layer is below the upper substrate layer and above the lower substrate layer; and
wherein said template is adapted to contain and determine the shape of a carbon nanotube as the carbon nanotube is created.

102. (previously presented) The process of claim 101, wherein the metal layer comprises patterned lines.

103. (previously presented) The process of claim 101, wherein the metal layer comprises a blanket deposit.

104. (previously presented) A carbon nanotube penetrating an upper substrate layer, a metal layer, and a lower substrate layer,
wherein the metal layer is below the upper substrate layer and above the lower substrate layer; and

wherein said carbon nanotube has been created in a template such that the shape of the carbon nanotube conforms to the shape of the template.

105. (previously presented) The process of claim 104, wherein the metal layer comprises patterned lines.

106. (previously presented) The process of claim 104, wherein the metal layer comprises a blanket deposit.

107. (previously presented) A carbon nanotube including a discontinuity, whereby there are two different conducting regions, one on either side of the discontinuity, and whereby the carbon nanotube comprises a diode.

108. (previously presented) The carbon nanotube of claim 107, wherein said carbon nanotube is in a substrate.

109. (previously presented) The carbon nanotube of claim 108, wherein said carbon nanotube further comprises:
an integrated source electrode; and
an integrated drain electrode.

110. (previously presented) An electronic device, comprising:
a first terminal;
a second terminal;
a substrate comprising a template structure extending between said first terminal and said second terminal;
a carbon nanotube formed within the template structure, wherein said carbon nanotube has at least one discontinuity therein, wherein the at least one discontinuity provides a first region and a second region, wherein the first region's conductivity differs from the second region's conductivity, wherein the first region is electrically connected to said first terminal, and wherein the second region is electrically connected to said second terminal.

111. (previously presented) A patterned array of carbon nanotubes in a substrate, wherein the carbon nanotubes are interconnected.

112. (previously presented) A patterned array of carbon nanotubes, wherein the carbon nanotubes are located at selected locations in a substrate, wherein the locations of the carbon nanotubes correspond to the locations of templates in a patterned array of templates in a substrate.

113. (previously presented) Two carbon nanotubes in a substrate comprising:
a first carbon nanotube;
a second carbon nanotube;

wherein said second carbon nanotube has a shape including at least two different diameters along said second carbon nanotube's vertical axis; and
wherein said first carbon nanotube is in electrical connection with said second carbon nanotube at a contact point such that said first carbon nanotube and said second carbon nanotube are interconnected.

114. (previously presented) Two carbon nanotubes in a substrate comprising:
a first carbon nanotube;
a second carbon nanotube; and
wherein said first carbon nanotube and said second carbon nanotube are vertically stacked and in electrical connection such that they are interconnected.

115. (previously presented) A vertically oriented carbon nanotube, wherein said vertically oriented carbon nanotube is created in a substrate, wherein said vertically oriented carbon nanotube includes a plurality of discontinuities along said vertically oriented carbon nanotube, wherein said vertically oriented carbon nanotube comprises a plurality of CNMEDs.

116. (previously presented) A CNMED comprising:
at least one vertically oriented carbon nanotube; and
at least one horizontal interconnect layer comprising horizontal conductive-only carbon nanotubes, wherein the horizontal conductive-only carbon nanotubes electrically connect said vertically oriented carbon nanotube.